REMARKS

Claims 1-13 are all the pending claims in the application.

Claims 1-6 and 8-13 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tang et al. (U.S. Patent Application Publication No. 2003/0206442 A1; hereinafter "Tang"). Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of M-Systems' article in Home Toys E-Magazine "One Chip Does it All" (hereinafter "M-Systems"). In response to the claim rejections, Applicant submits the arguments below in traversal.

Applicant respectfully submits that claim 1 is believed to be patentable because the Examiner's characterization of certain elements of Tang as corresponding to the claimed cache module and the main control unit, is inconsistent and does not support the rejection of claim 1. For example, Tang fails to disclose or suggest:

> a cache module for accessing a designated memory address of the serial flash in response to a command received from a main control unit through a system interface unit, and reading or writing data required by the main control unit in a read or write operation

(Emphasis added).

In the Final Office Action, the Examiner alleges that the cache control logic disclosed in the Abstract of Tang corresponds to the claimed cache module. See pg. 3. In the detailed description, this cache control logic refers to either the control logic unit 320 or the main control logic unit 355 inside the control logic unit 320. The Examiner then alleges that the aforementioned main control logic unit 355 corresponds to the claimed main control unit, when the main control logic unit 355 was already cited as corresponding to the claimed cache module.

Even if the Examiner intended to allege that the control logic unit 320 corresponds to the claimed cache module, the Examiner's characterization is still unsupportable. Claim 1 recites a cache module for accessing a designated memory address of the serial flash in response to a command received from a main control unit through a system interface unit. Therefore, the Examiner's characterization would necessarily require the control logic unit 320 (corresponding to the cache module) to receive a command from itself, i.e., the main control logic unit 355 which is a component of the control logic unit 320.

Further, if one is to assume that the Examiner intended to allege that the buffer logic control unit 330 corresponds to the claimed cache module, the Examiner's characterization is even still not supportable because the buffer logic control unit 330 does not access a designated memory address of the serial flash, as recited in claim 1. Instead, the main control logic unit 355 accesses the buffer region 310 which is described as being FIFO or RAM-type memory. See paragraph 23. The cache module, however, cannot correspond to the main control logic unit 355 for the reasons mentioned above.

Moreover, Tang fails to disclose or suggest:

> a serial flash controller with a boot loader for allowing system booting to be performed by reading boot codes written on the serial flash, storing the boot codes in a buffer and immediately transmitting the boot codes to the main control unit when the main control unit requires the boot codes.

Although the Examiner cites the NAND flash memory control unit 350 as corresponding to the claimed serial flash controller, the NAND flash memory control unit 350 does not store the boot codes in a buffer and immediately transmit the boot codes to the main control unit when the

main control unit requires the boot codes, as recited in the claim. Rather, it is the buffer region 310 which stores the boot codes. See paragraph 9.

Therefore, for at least the above reasons and for the reasons previously submitted in the January 23, 2006 Amendment, claim 1 is believed to be patentable.

For reasons similar to those submitted for claim 1, claim 6 is believed to be patentable.

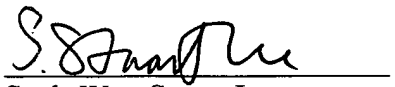
As for claim 8, Applicant submits that claim 8 is believed to be patentable because Tang fails to disclose or suggest searching the memory address from a tag-storing unit of the controller in response to the received read command, as recited in the claim. In the Final Office Action, the Examiner appears to take the position that Tang inherently discloses the aforementioned feature of claim 8 because Tang does not explicitly disclose searching the memory address from a tag-storing unit. Tang, however, discloses a buffer region 310 and there is nothing to suggest that a memory address could not be searched from the buffer region 310 instead of searching for the memory address in a unit of the control logic unit 320. Therefore, Tang does not disclose searching the memory address from a tag-storing unit of the controller.

Claims 2-5 and claims 9-13, which depend from claims 1 and 8, respectively, are believed to be patentable for at least the reasons submitted for their respective base claims.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Seok-Won Stuart Lee
Limited Recognition No. L0212

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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